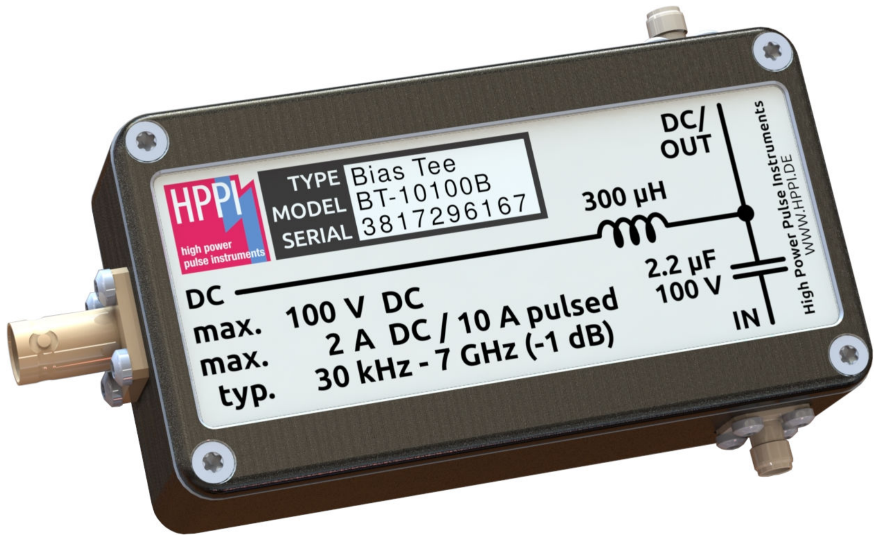
100 V, 10 A, 30 kHz – 7 GHz High Voltage Bias Tee BT-10100B

Advanced TLP/HMM/HBM Solutions



1 Features

- High voltage 30 kHz to 7 GHz (−1 dB S21) bias tee
- 100 V DC bias voltage
- DC input bias current: max. 2 A DC and max. 10 A pulsed at 100 ms pulse width and 1 % duty cycle
- Typ. 0.4 Ω DC resistance (port 3 to port 2)
- SMA 50 Ω pulse input and 50 Ω DC/pulse output
- BNC DC input
- Suitable for high-current TLP, VF-TLP and HMM
- Size: 130.6 mm x 77.6 mm x 31 mm
- Lab safety requirement: interlock operation above an operation voltage of 40 V needed to avoid life-endangerment risks.

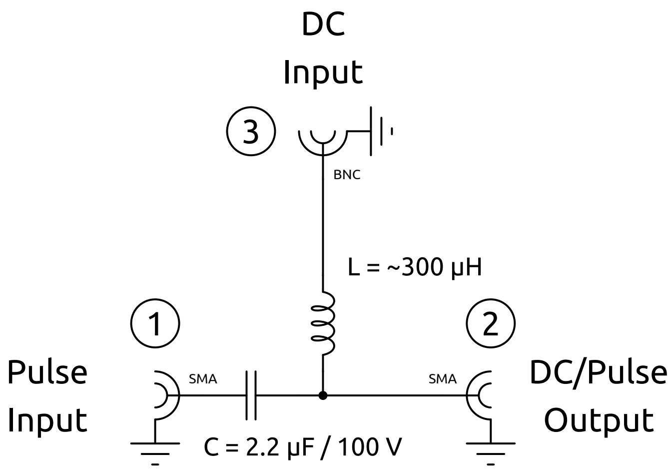


Figure 1: Simplified schematic diagram

2 Description

The BT-10100B is used for DC biased TLP, VF-TLP, HMM or general RF measurements of high voltage and power devices in the time domain or frequency domain. The DC voltage or current is applied to the DC input (port 3). The TLP output (pulse force) is connected to the pulse input (port 1). The DUT or DUT pulse force line is connected to the DC/pulse output (port 2). The BT-10100B features a lower cut-off frequency of 30 kHz at high bandwidth of 7 GHz. Fig. 1 shows the simplified schematic diagram.

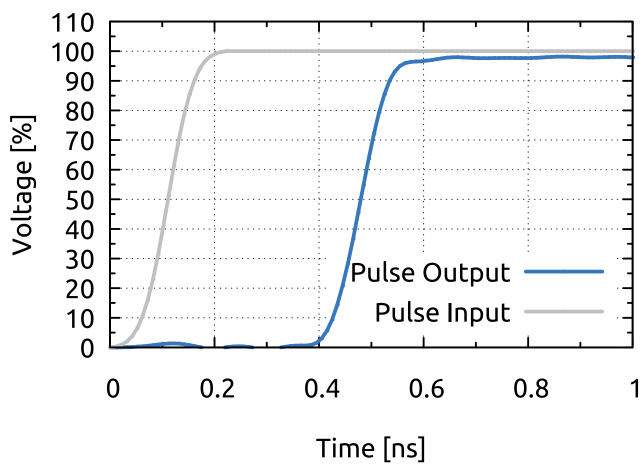


Figure 2: Step response of the bias tee at the pulse output (port 2) with input pulse rise time of 100 ps at the pulse input (port 1).

2.1 Electrical Characteristics

Fig. 2 shows the step response[1] from port 1 to port 2 at 100 ps input pulse rise time. The time delay of the output signal is about 0.4 ns.

Fig. 3 shows the typical insertion loss from port 1 to port 2.

[1]calculated based on measured S-parameters in the range from 300 kHz to 9 GHz and excitation input pulse rise-time of 100 ps.

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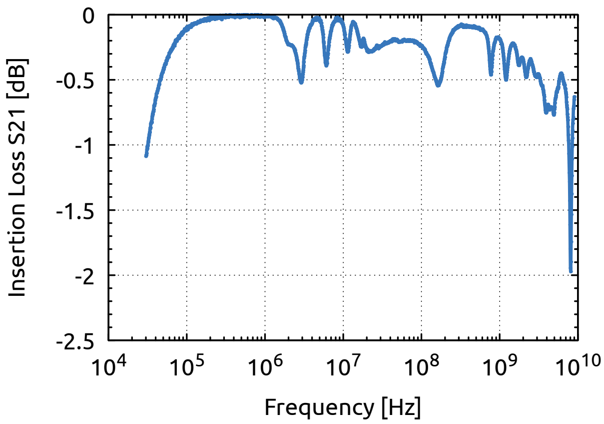

Figure 3: Measured insertion loss S21: pulse input to DC/pulse output in [dB]. Measurement condition: DC input port 3 terminated with 50 Ω.

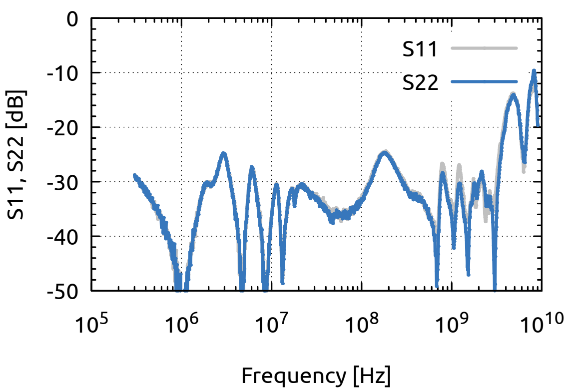

Figure 4: Measured reflection coefficients S11, S22: pulse input, DC/pulse output in [dB]. Measurement condition: DC input port 3 terminated with 50 Ω.

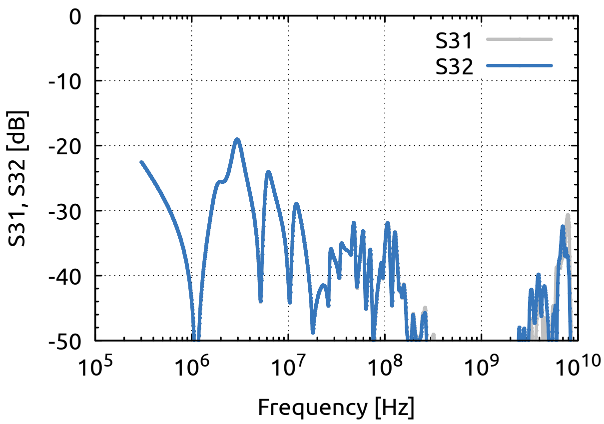

Figure 5: Measured isolation S31, S32: pulse input, DC/pulse output to DC input in [dB]. Measurement condition: DC input port 3 terminated with 50 Ω.

3 Application Note

3.1 SMU Control Loop Instabilities

Sometimes a bias tee is used in the measurement setup to set the DC bias voltage or current of the DUT using a SMU.

For typical TLP measurements the 50 Ω bias tee must have a lower cut-off frequency of around 30 kHz for large pulse width and an upper cut-off frequency in the range of several GHz to ensure a fast pulse rise time. This results in quite large L and C values inside the bias tee.

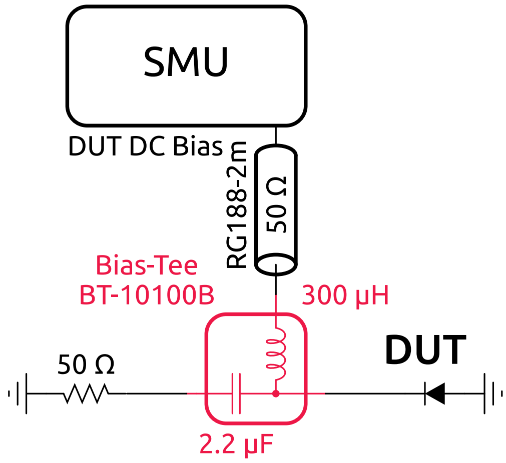

Figure 6: Typical bias tee application

Fig. 6 shows the equivalent model of a typical bias tee application. The SMU has to deal with a very extreme impedance situation at its output. First a shunt capacitance of 200 pF is caused by the 2 m long 50 Ω coaxial cable. Then a large inductance of 300 µH and further a 2.2 µF capacitor connected in series with 50 Ω is shunted by the DUT.

This extreme load impedance at the SMU output may have strong impact on the control loop of the SMU. Depending on the phase margin of the SMU open-loop gain, the SMU output may become unstable. Unexpected damage of the DUT may happen because of a sudden SMU output runaway or high voltage oscillations. If the DUT impedance is changing in a wide range from short circuit to high impedance or representing a nonlinear characteristic, the SMU stability will be dependent on the DUT impedance in the measurement setup. Note: the situation may change significantly in case of a 4-wire (Kelvin) setup.

Please investigate the stability of the SMU with a separate test setup as shown in Fig. 6, check the SMU manual and/or contact the SMU vendor.

3.2 Increase SMU Control Loop Stability

A simple but very effective countermeasure to increase the SMU control loop stability is to connect a resistor *R* directly at the output of the SMU, as shown in Fig. 7.

The value of the resistor should be as large as possible. Several hundred Ω to kΩ may be sufficient.

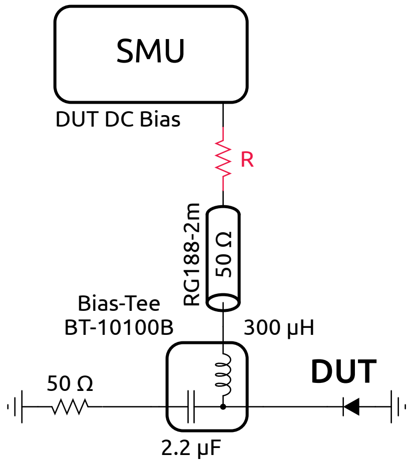

Figure 7: Increase SMU output stability with a resistor *R* connected in series

3.3 Laboratory Safety Requirement

Interlock operation above an operation voltage of 40 V needed to avoid life-endangerment risks.

4 Dimensions

Fig. 8 shows the enclosure dimensions of the BT-10100B.

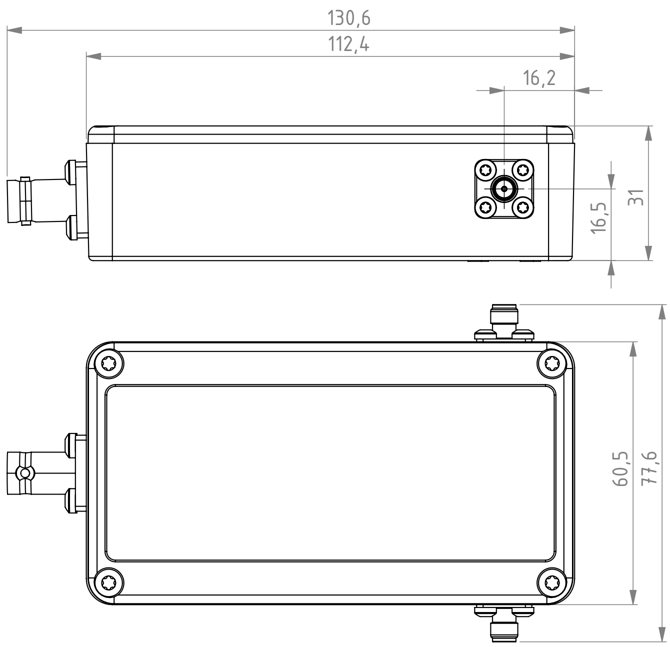

Figure 8: Physical dimensions of the BT-10100B in [mm]

On the bottom side the enclosure has two M4 threads and two Ø 4 mm dowel holes for fixation of the BT-10100B in the measurement setup (Fig. 9).

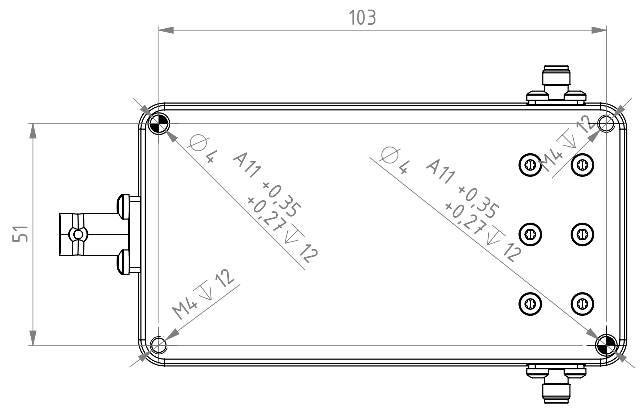

Figure 9: Bottom side fixation threads and dowel holes. All dimensions in [mm].

5 Ordering Information

Pos.	Description	Part No.
01	100 V, 10 A, 30 kHz – 7 GHz High Voltage Bias Tee	BT-10100B

General

The product data contained in this data-sheet is exclusively intended for technically trained staff. You and your technical departments will have to evaluate the suitability of the product for the intended application and the completeness of the product data with respect to such application. Our products are solely intended to be commercially used internally and should not be sold to consumers. This data-sheet is describing the specifications of our products for which a warranty is being granted by HPPI GmbH. Any such warranty is granted exclusively pursuant the terms and conditions of the respective supply agreement. There will be no guarantee of any kind for the product and its specifications. For further information on technology, specific applications of our product, delivery terms, conditions and prices please contact HPPI:

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